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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,917	07/23/2003	Shahram Mostafazadeh	NSC1P194D1/P04836D1	9491
22434	7590	08/25/2004	EXAMINER	
BEYER WEAVER & THOMAS LLP			ROSE, KIESHA L	
P.O. BOX 778			ART UNIT	
BERKELEY, CA 94704-0778			PAPER NUMBER	

2822

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/625,917

Applicant(s)

MOSTAFAZADEH, SHAHRAM

Examiner

Kiesha L. Rose

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) ____ is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. ____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 7/23/2003.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

This Office Action is in response to the filing of the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6,8,11,12 and14 are rejected under 35 U.S.C. 102(e) as being anticipated by Shinohara (U.S. Patent 6,358,778)

Shinohara discloses a semiconductor device (Fig. 4a) that contain a first die (4) with a conductive side, a plurality of lead post (2) having equal space and pitch and having oversized contact pads (12) on a bottom surface of the integrated circuit with a large diameter, wherein the conductive side of the first die faces the plurality of lead posts, the conductive side of the die comprises a plurality of spaced apart conductive pads which are mechanically and electrically connected to the lead posts, an encapsulant material (7) encapsulating the first die and an end of the lead posts adjacent to the conductive side of the die and has a top and bottom surface and the oversized contact pads are formed on the bottom part, where the conductive side of the

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die is mechanically and electrically connected to the lead posts, where the lead posts have a square cross section and lengths that are perpendicular to the conductive side of the die.

Claims 1-8,11,12,14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Satsu et al. (U.S. Patent 6,225,418).

Satsu discloses a semiconductor device (Figs. 2 and 4b) that contain a first die (1) with a conductive side, a plurality of lead post (9/5) having equal space and pitch and having oversized contact pads (9) on a bottom surface of the integrated circuit with a large diameter, wherein the conductive side of the first die faces the plurality of lead posts, the conductive side of the die comprises a plurality of spaced apart conductive pads which are mechanically and electrically connected to the lead posts, an encapsulant material (15) encapsulating the first die and an end of the lead posts adjacent to the conductive side of the die and has a top and bottom surface and the oversized contact pads are formed on the bottom part, where the conductive side of the die is mechanically and electrically connected to the lead posts, where the lead posts have a square and round cross section and lengths that are perpendicular to the conductive side of the die.

Claims 1-5 and 7-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (U.S. Patent 6,258,626).

Wang discloses a semiconductor device (Fig 1) that contain a first die (110) with a conductive side, a plurality of lead post (124/112) having equal space and pitch and having oversized contact pads (112) on a bottom surface of the integrated circuit with a

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large diameter, wherein the conductive side of the first die faces the plurality of lead posts, the conductive side of the die comprises a plurality of spaced apart conductive pads (above lead posts) which are mechanically and electrically connected to the lead posts, a second die (130) with a conductive side and a side opposite the conductive side wherein the side opposite the conductive side is connected to a side opposite the conductive side of the die, wirebonding (132) connected between the conductive side of the second die and at least one lead post of the plurality of lead posts, an encapsulant material (140) encapsulating the first die, second die and an end of the lead posts adjacent to the conductive side of the die and has a top and bottom surface and the oversized contact pads are formed on the bottom part, where the conductive side of the die is mechanically and electrically connected to the lead posts, where the lead posts has a round cross section and lengths that are perpendicular to the conductive side of the die.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9, 10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Shinohara in view of Wang.

Shinohara discloses all the limitations except for a second die connected to the first die. Whereas Wang discloses a semiconductor package (Fig. 1) that contains a first die (110) with a conductive side, a second die (130) with a conductive side and a side opposite the conductive side of the first die wherein the side opposite the conductive side connected to a side opposite the conductive side of the first die, lead posts (112/124) a wirebonding (132) connected between the conductive side of the second die and at least one of the lead posts, and encapsulate (140) encapsulating the first and second die, lead post and wirebonding. A second die is connected to the first die for flip chip connection. (Column 1, lines 12-14) Therefore it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Shinohara by incorporating a second die connected to the first die for flip chip connection as taught by Wang.

Claims 9,10 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Satsu in view of Wang.

Satsu discloses all the limitations except for a second die connected to the first die. Whereas Wang discloses a semiconductor package (Fig. 1) that contains a first die (110) with a conductive side, a second die (130) with a conductive side and a side opposite the conductive side of the first die wherein the side opposite the conductive side connected to a side opposite the conductive side of the first die, lead posts (112/124) a wirebonding (132) connected between the conductive side of the second die and at least one of the lead posts, and encapsulate (140) encapsulating the first and second die, lead post and wirebonding. A second die is connected to the first die for flip

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chip connection. (Column 1, lines 12-14) Therefore it would be obvious to one of ordinary skill in the art at the time the invention was made to modify the device of Satsu by incorporating a second die connected to the first die for flip chip connection as taught by Wang.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
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